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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,004	11/29/2001	Jack L. Granato	H0001962 US	9718

7590 07/30/2004

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,004	GRANATO ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Long et al. (USPN 4974144). As appears in claim 9, Long et al. discloses first means for running an application program for a user interface to control the operation of the devices and manipulate data manifesting the operation of the devices; a first data bus for exchanging data between said first means and a signal processor; means connected to said first data bus for storing said data for subsequent use by said signal processor; a local bus that connects the devices; a gate array for exchanging data between said signal processor and the devices; means associated with each device for controlling the exchange of data between said gate array and a device over said local bus and storing data for use by said gate array in column 7, lines 1-11, 54-68.

3. As per claim 10, Long et al. discloses said means associated with each device comprises means for generating a signal that manifests that defective communication between the device and the local bus in column 43, line 30 – column 44, line 13.

4. As per claim 11, Long et al. discloses running an application program for a user interface to control the operation of the devices and manipulate data manifesting the operation of the devices; exchanging data between said first means and a first signal

processor on a first data bus for; storing said first data for subsequent use by said first signal processor; connecting the devices over a local bus; exchanging data between said signal processor and the devices using a second signal processor; and controlling the exchange of data between said second signal processor and each device over said local bus and storing data on said local bus for use by said second signal processor in column 7, lines 1-11, 54-68.

5. As per claim 12, Long et al. discloses wherein the second signal processor comprises a gate array column 7, lines 1-11.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. in view of Ogilvie et al. (USPN 5854908A). As appears in claim 1, Long et al. discloses a first computer comprising a first bus, a first signal processor and a user interface for entering instructions and running an application program to receive data from each device, provide instructions to each device and analyze the operation of each device; a bus control logic unit controlling data flow by each device to the second bus; a second signal processor connected to read from and write data to the first bus; a gate array responsive to signals from said second signal processor for reading from and writing data to the second signal processor and each bus control logic unit to control the

operation of each device in response to instructions generated from said first computer; and a memory for storing data while either the first signal processor or the second signal processor is performing operations on previous data in said memory in column 7, lines 1-11, 54-68.

Long et al. fails to explicitly state said first bus operating at a first rate and a second bus that operates had a second array [at a second rate] different from said first rate.

Ogilvie et al. discloses this limitation in column 1, lines 54-63.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first bus operating at a first rate and a second bus that operates had a second array [at a second rate] different from said first rate. A person of ordinary skill in the art would have been motivated to have said first bus operating at a first rate and a second bus that operates had a second array [at a second rate] different from said first rate because buses operating at different rates allows a computer system to transfer certain data at faster rates and certain data at slower rates.

8. As per claim 2, Long et al. discloses each bus control logic unit comprises means for storing data for its respective device from said gate array while said second signal processor is unavailable for utilizing said data column 9, lines 37-45.

9. As per claim 3, Long et al. discloses said gate array waits for a bus control logic unit to signify that data has been completely read from or to the gate array and the second signal processor waits for said acknowledgement before providing data to or receiving data from said gate array in column 36, line 43 – column 37, line 2.

10. As per claim 4, Long et al. discloses said second signal processor stores data from said gate array in said memory for use by said first signal processor in column 7, lines 54-68.

11. As per claim 5, Long et al. discloses each bus control logic unit comprises means for storing data control instructions from said gate array for its respective device while said second signal processor is unavailable for utilizing said data in column 9, lines 37-45.

12. As per claim 6, Long et al. discloses said bus control logic unit provides a signal to say [said] gate array to cause said first computer to identify than [that] a bus connection with a device is defective in column 43, line 30 – column 44, line 13.

13. As per claim 7, Long et al. discloses running an application program on a first computer; using a first data bus on said first computer for exchanging data between said first computer and a signal processor; storing said data in a memory on said first bus for subsequent use by said signal processor; exchanging data between said signal processor and a gate array; exchanging gate array produced data with logic units, each controlling the exchange of data between a respective device and storing data produced by the devices with said logic devices until the gate array is available to use said data in column 7, lines 1-11, 54-68.

Long et al. fails to explicitly state a bus that operates as [at] a different rate and different protocols then [than] the first data bus.

Ogilvie et al. discloses this limitation in column 1, lines 54-63.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a bus that operates as [at] a different rate and different protocols then [than] the first data bus. A person of ordinary skill in the art would have been motivated to have a bus that operates as [at] a different rate and different protocols then [than] the first data bus because buses operating at different rates allow a computer system to transfer certain data at faster rates and certain data at slower rates. Buses having different protocols allow data to be transferred to different devices throughout the computer system.

14. As per claim 8, Long et al. discloses generating a signal from one of the logic units to indicate that a bus connection to its respective device is defective in column 43, line 30 – column 44, line 13.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100